AMENDMENTS TO THE SPECIFICATION

Please amend specification paragraph **[0035]** as follows:

--**[0035]** FIG. 2 shows a side view, of the prior art chip scale package 2. Chip 4 has ~~connection pads~~sockets 20A-20C. Solder balls 3A-3C are interposed between sockets ~~21A-21C~~20A-20C and conductive PCB contacts 22A-22C to form respective current pathways between PCB 1 and chip 4. The conductive PCB contacts 22A-22C are in electrical contact with PCB wiring traces 24A-24C connecting chip 4 with other components (not shown) of PCB 1. The sockets ~~21A-21C~~20A-20C are each formed to include, for example, a conductive pathway formed by an adhesion layer 25 bonded to wafer 26 and UBM 27. BCB layer 28 and passivation layer 29 define sockets 20A-20C in areas apart from UBM 27.--

Please amend specification paragraph **[0039]** as follows:

--**[0039]** Sockets 37A, 37B may be formed by multiple processes; for example by screen printing the adhesion layers 49A, 49B, onto wafer 50, followed by liquid or vapor deposition of passivation layer 44 to a uniform thickness at interface 51. BCB layer 45 is applied through a mask to passivation layer 44. The masked application of BCB layer 45 leaves areas of passivation layer 44 exposed, including the areas of the passivation layer covering adhesion layers 49A-C. Lithographic etching of passivation layer 44, where passivation layer 44 is unprotected by the masked application of BCB layer 45, removes the exposed portions of passivation layer 44. As a result, adhesion layers 49A-C are exposed and available to receive sputtered UBM layers ~~52A-52C~~42A-42C. A discrete and isolated electric pathway is formed, for example, between wafer 50, adhesion layer 49A, UBM layer 42A, solder bar 41, trace 46A, and via 47A.—

Please delete specification paragraph **[0040]**.

Please amend specification paragraph **[0041]** as follows:

--**[0041]** FIG. 5 is a top view of wafer package 40. Solder balls 43, 43A-E connect PCB 48 to data traces 54, 54A-E and sockets ~~55~~37C, 55A-E on wafer 50. Power traces 46A, 46B, solder bars 41, 42 and sockets ~~47A, 47B~~37A, 37B form

respective power circuits. One or more of the solder balls 43, 43A-E may optionally be replaced by solder bars to accommodate greater current and/or heat flow, improve package reliability, or to simplify the design and/or manufacture of wafer package 40.--

Please amend specification paragraph **[0042]** as follows:

--**[0042]** FIG. 6 is a top view of PCB 60, which may be used with a combination of solder balls and solder bars. PCB 60 contains a plurality of semi-spherical solder ball traces 61 and rectangular solder bar traces 62A-D. Traces 62A-D may be formed by known processes, such as screen printing or stenciling of gold, copper, aluminum, or other conductor materials onto PCB 60. Solder bar traces 62A-D and solder ball traces 61 each present solder-bonding surfaces. It will be appreciated that the elements of PCB 60 may be arranged and deployed for use as PCB ~~6048~~ shown in FIG. 5, or in any other manner that is effective to implement circuit requirements on PCB 60.--